	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	795	(input adj1 buffer) and (transfer adj1 gate) and (control adj1 circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/25 13:10	
2	BRS	L2	103	1 and (interface adj1 circuit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/25 13:27	
3	IS&R	L3	326	(257/500).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/25 13:44	
4	IS&R	L4	481	(257/365).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/25 13:57	

	Error Definition	Errors
1		0
2		0
3		0
4		0

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	IS&R	L5	359	(257/393).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/25 14:08	
6	IS&R	L6	64	(257/271).CCLS.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/09/25 14:08	

	Error Definition	Errors
5		0
6		0